REMARKS/ARGUMENTS

Reconsideration of the application is requested.

Claims 1-3 and 5-13 remain in the application.

In the section entitled "Claim Rejections - 35 USC § 103" on pages 2-7 of the above-mentioned Office action, claims 1-3 and 5-13 have been rejected as being unpatentable over Shiga (US 5,416,660) in view of Chrysostomides et al. (US 5,646,434) and Takamoto et al. (US 5,079,612) under 35 U.S.C. § 103(a).

As will be explained below, it is believed that the claims were patentable over the cited art in their original form and the claims have, therefore, not been amended to overcome the references.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful.

Claim 1 calls for, inter alia:

> a first conductor track running outside said semiconductor chip, said first conductor track being connected to said terminal for the signal;
>
> ...

a further conductor track running outside said semiconductor chip, said further conductor track being connected to said second conductor track, said further conductor track surrounding said semiconductor chip, said further conductor track crossing said first conductor track, defining a crossing location, and said further conductor track crossing said second conductor track; and

an electrostatic discharge protection element for carrying an electrostatic discharge away from said terminal for the signal and to the supply potential, said electrostatic discharge protection element being disposed outside of said semiconductor chip, said electrostatic discharge protection element being connected outside of said semiconductor chip to said further conductor track and to said first conductor track, said electrostatic discharge protection element being disposed close to said crossing location.

Shiga shows a microwave circuit. However, Shiga does not disclose in which way the ground potential can be delivered from one of the power supply terminals 6 to the diode 9, which is part of the protection circuit.

In the invention of the instant application, the further conductor track (3) is a conductor track running outside the semiconductor chip. Chrysostomides et al. do not show a conductor track that runs outside the chip. The Examiner has argued on page 7 of the Office aciton that the broad recitation of the claim does not exclude the further conductor track 23 from being an integrated conductor track. Applicant is uncertain what claim the examiner has referred to. The claims of Chrysostomides et al. are not relevant in this respect since they do not positively mention this feature, and

claim 1 of the instant application calls for "a further conductor track running outside said semiconductor chip."

It is noted with regard to pages 2-4 of the Office action, that the examiner has not shown that the prior art teaches that a further conductor track surrounding the semiconductor chip would be disposed outside the chip. The conductor track 23 of Chrysostomides et al. is disposed inside the chip. The conductor tracks 22, 21 of Takamoto et al. are also disposed inside the chip. All elements shown in Fig. 1 of Takamoto et al. are meant to be disposed on a single die of a semiconductor chip. The text in column 5, lines 13 to 28 of Takamoto et al. relates to the chip level description of the circuit shown in Fig. 1 of Takamoto et al. The internal circuit block 1 (see Fig. 2) occupies the major part of the chip area. The protective elements 16 are connected between the main ground line 22 and the ground line 42 adjacent the block 3 within the wiring domain of the internal circuit block 1, from which it can be concluded that all elements described so far are located on the semiconductor chip. Since the terminals 104, 105, 106, etc, are terminals of the chip, the circuit in Fig. 1 will be contained in a semiconductor chip.

Consequently, no prior art reference shows a conductor track surrounding the chip, which is disposed outside the chip and

which is connected to an electrostatic discharge protection element.

According to claim 1 of the instant application, a crossing location is defined between the further conductor track (running outside the semiconductor chip) and the first conductor track (also running outside the semiconductor chip). The first conductor track is connected to the terminal for the signal. Thus, the feature of "crossing" relates to a conductor track (i.e. the first conductor track), which is connected to a signal line. The Examiner has mentioned bonding wires 6, 9 of Chrysostomides et al., which cross the conductor track 23 of Chrysostomides et al. This means that the Examiner has drawn a parallel between the further conductor track of the invention of the instant application and the conductor track 23 of Chrysostomides et al. and the first conductor track of the invention of the instant application and the bonding wires 6, 9 of Chrysostomides et al. However, bonding wires 6, 9 of Chrysostomides et al. carry supply potentials while the first conductor track of the invention of the instant application is defined as being connected to a terminal for a signal, which means that it actually will carry a signal to be processed. Applicant therefore believes that the bonding wires 6, 9 of Chrysostomides et al. cannot be used to argue obviousness of

the crossing location of claim 1 of the instant application, because the crossing location of the invention of the instant application is defined between the further conductor track and the first conductor track, which is a conductor track for a signal (rather than for a supply potential for which bonding wires 6, 9 of Chrysostomides et al. are intended).

In summary, none of the references teaches providing a further conductor track outside a semiconductor chip surrounding the semiconductor chip, an electrostatic discharge protection element connected to the further conductor track outside the chip and surrounding the chip, a crossing location between the further conductor track and the first conductor track which must be arranged outside the chip, and the first conductor track being connected to a terminal for a signal. Since all the above features are not shown in the prior art, and references Chrysostomides et al. and Takamoto et al. provide all elements on the chip, Applicant believes that the invention of the instant application is patentable over the prior art.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claim 1. Claim 1 is, therefore, believed to be patentable over the art and since

all of the dependent claims are ultimately dependent on claim 1, they are believed to be patentable as well.

In view of the foregoing, reconsideration and allowance of claims 1-3 and 5-13 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate a telephone call so that, if possible, patentable language can be worked out.

If an extension of time for this paper is required, petition for extension is herewith made. Please charge any fees which might be due with respect to 37 CFR Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,

Yonghong Chen
Reg. No. 56,150

Yonghong Chen
For Applicant

YC

August 29, 2005

Lerner and Greenberg, P.A.
Post Office Box 2480
Hollywood, FL 33022-2480
Tel: (954) 925-1100
Fax: (954) 925-1101